SPECIFICATION

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CONTENT ADDRESSABLE MEMORY WITH PFET PASSGATE SRAM CELLS

Background of the Invention

[0001] Field of the Invention

[0002] The present invention relates generally to An SRAM based CAM (Content Addressable Memory) cell with PFET passgate SRAM cells which results in a smaller cell size because of a more balanced number of PFET devices and NFET devices.

[0003] Discussion of the Prior Art

[0004] CAM (Content Addressable Memory) is the main component of internet routers and switches. CAM can also be used in many other applications such as pattern recognition and cryptography. A full ternary CAM cell in general consists of two memory bits and the compare logic. The full ternary CAM cell allows full array search with per bit masking. The memory bits may be provided by DRAM cells or SRAM cells. DRAM based CAM is smaller, but requires the more complex DRAM process and the refresh operation to maintain the data. SRAM based CAM is larger, but the fabrication process is cheaper and the design is simpler. A typical SRAM based CAM cell consists of 16 devices, with 4 PFETs providing the SRAM cell pull ups, and with 12 NFETs for the SRAM cells and for the compare logic. The size is very large, about 4 - 5 times the size of a typical 6T SRAM cell. A typical 6T SRAM cell consists of 2 pull up PFETs, 2 pull down NFETs and 2 passgate NFETs.

[0005] Figure 1A is a circuit schematic, with a truth table of operation, of a prior art full ternary CAM cell with NFET passgates which comprises 16 transistors, 4 PFETs and 12 NFETs.

[0006] Figure 1B is a circuit layout of the prior art full ternary CAM cell of Figure 1A and illustrates further details of the prior art design at the 0.13 um node of CMOS technology, which is shown for circuit area comparison purposes with the full ternary CAM cell with PFET passgates of the present invention.

Brief Summary of the Invention

[0007] The present invention provides a Content Addressable Memory (CAM) with PFET passgate SRAM cells which results in a smaller cell size because of a more balanced number of 8 PFET devices and 8 NFET devices. Moreover, the use of PFET passgates allows the size of the SRAM cell pulldown devices to be reduced to a minimum size. The PFET passgates also consume less power as PFET off currents are generally much smaller than NFET off currents. The ratio is about 1 to 20. The standby power is further reduced because the SRAM pull down NFETs are smaller with the PFET passgates. With PFET passgates, the SRAM read/write bit lines can also be biased to some voltage level between GND and VDD, instead of to VDD as in the prior art. For example, if the read/write bit lines are biased at one half VDD, the SRAM read/write power can be lowered by 3/4. Thus the standby power dissipation and the read/write power are both reduced.

Brief Description of the Several Views of the Drawings

[0008] The foregoing objects and advantages of the present invention for a content addressable memory (CAM) with PFET passgate SRAM cells may be more readily understood by one skilled in the art with reference being had to the following detailed description of a preferred embodiment thereof, taken in conjunction with the accompanying drawings wherein like elements are designated by identical reference characters throughout the several views, and in which:

[0009] Figure 1A is a circuit schematic, with a truth table of operation, of a prior art full ternary CAM cell with NFET passgates.

[0010] Figure 1B is a circuit layout of the prior art full ternary CAM cell of Figure 1A.

[0011] Figures 2A and 2B are respectively a circuit schematic, with a truth table of operation, and a circuit layout of a preferred embodiment of a full ternary CAM cell with PFET passgates pursuant to the present invention.

[0012] Figure 2C shows the metal wiring of the design of Figure 2B.

[0013] Figure 2D corresponds generally to Figure 2B, and illustrates further details and dimensions of the new design at the 0.13 um node of CMOS technology.

Detailed Description of the Invention

[0014] The present invention provides a CAM cell layout with PFET passgate SRAM cells which allows the CAM cell area to be reduced to about 20% the size of a typical prior art SRAM cell with NFET passgates. The more optimized CAM cell layout is a result of a more balanced design of 8 PFETs and 8 NFETs in the overall circuit.

[0015] The layout layers and other references in the Figures are shown as:

[0016] RX: active silicon

[0017] PC: Polysilicon conductor

[0018] NW: N-type well for the PFET

[0019] CA: Contacts, between PC or RX and M1

[0020] M1: 1st layer of metal

[0021] V1: Via connection between M1 and M2

[0022] M2: 2nd layer of metal

[0023] V2: Via connection between M2 and M3

[0024] M3: 3rd layer of metal

[0025] VDD: power supply

[0026] GND: ground

[0027] EC: electrical connector by M1

[0028] WL: wordline

[0029] ML: matchline

[0030] Figures 2A and 2B are respectively a circuit schematic, with a truth table of operation, and a circuit layout of a preferred embodiment of a full ternary CAM cell with PFET passgates pursuant to the present invention.

[0031] Referring to Figure 2A, the full ternary CAM cell with PFET passgates includes a bottom SRAM 20 consisting of 6 devices, 2 NFET pull down devices N1, N2, 2 PFET pull up (to VDD) devices P1, P2, and 2 PFET passgate devices, a passgate left device PL and a passgate right device PR.

[0032] The full ternary CAM cell further includes a top SRAM 22 consisting of 6 devices which form a duplicate of the bottom SRAM circuit, with the 6 devices being reversed from left to right with respect to the bottom SRAM circuit. Thus, the top SRAM includes 2 NFET pull down devices N1, N2 reversed left to right, 2 PFET pull up (to VDD) devices P1, P2 reversed left to right, and 2 PFET passgate devices reversed left to right, a passgate left device PL (which is actually on the right side) and a passgate right device PR (which is actually on the left side).

[0033] The full ternary CAM cell further includes a middle exclusive OR (XOR) gate 24 consisting of 4 NFET devices N3, N4, N5, N6.

[0034] The full ternary CAM cell includes 2 wordlines, WLA for the top SRAM 22 and WLB for the bottom SRAM 20, 2 bitlines, bitline left BL and bitline right BR, 2 searchlines, searchline left SL and searchline right SR, and a master data line ML.

[0035] The full ternary CAM cell operates in accordance with the truth table shown in Figure 1 wherein the 4 possible states are shown, in lines 1-4, of CELLA, the top SRAM connected to WLA, and CELLB, the bottom SRAM connected to WLB. The 4 states correspond respectively to the states 00 (DON'T CARE), 01 (ZERO), 10 (ONE), 11 (MISMATCH ALWAYS). It is noted that the truth table of Figure 2A is the same truth table of operation as the prior art CAM cell with NFET passgates as shown in Figure 1A.

[0036] Taking line 2 of the truth table as an example, wherein CELLA is 0 and CELLB is 1, this corresponds to device N3 being OFF and device N4 being ON. If SL is 0, and SR is 1, the search operation will result in a "MISS" condition or "MISMATCH" condition with the ML being pulled down. This means that the CAM cell data is 0 while the search is

for 1, and so the search is unsuccessful. On the other hand, if CELLA is 1 and CELLB is 0 as shown in line 3 of the truth table, the match line ML will not bepulled down when the same search bit is presented, with SL at 0 and SR at 1.

[0037] Assume phone numbers are listed under customer names, and the customer names are encoded into 100 bits. When these 100 bits of a customer name are presented to the CAM, and if all 100 bits are matched with the stored data, the ML will not be pulled down and the match signal staying high will access the corresponding entry of phone number.

[0038] If CELLA is 0 and CELLB is 0 as shown in line 1 of the truth table, then the CAM cell will not pull the ML down. The CAM data is thus "masked off" from the search operations.

[0039] Lines 1, 2, 3 of the truth table form the "ternary" states of the CAM cell. The fourth state with CELLA at 1 and cellB at 1 is not used in the search operations. When each bit can be independently "masked off", the CAM cell is referred to as a full ternary CAM cell. If the "masking" can be applied only to a group of more than 1 bit, the CAM cell is then not a "full ternary" CAM cell.

[0040] Figure 2B is a circuit layout of a preferred embodiment of a CAM cell with PFET passgates pursuant to the present invention. The bottom of Figure 2B shows the layout of the bottom SRAM 20 six devices N1, N2, P1, P2, PL, PR, which are shown as being formed at the intersections of first and second different active silicon regions RX1, RX2 with first, second and third different polysilicon conductors PC1, PC2, PC3 of the cell. The top of Figure 2B shows the layout of the top SRAM 22 six devices N1, N2, P1, P2, PL, PR which are also formed at intersections of second and third different active silicon regions RX2, RX3 with fourth, fifth and sixth different polysilicon conductors PC4, PC5, PC6. The middle of Figure 2B shows the layout of the exclusive OR gate 24 four devices N3, N4, N5, N6 which are also formed at intersections of the second active silicon region RX2 with third, sixth, seventh and eighth different polysilicon conductors PC3, PC6, PC7, PC8.

[0041] The bottom of Figure 2B shows the layout of the bottom SRAM 20 and shows a generally M shaped first active silicon region labeled RX1. A generally shallow U

shaped first polysilicon conductor labeled PC1 crosses the M shaped active silicon region RX1 twice at the two end legs thereof to form the gates of the devices PL, PR, wherein the top of the RX1 active silicon region forms the source of each of the devices PL, PR, and the bottom of the RX1 region forms the drain of each of the devices PL, PR.

[0042] Referring to the middle of Figure 2B, a second active silicon region labeled RX2 includes a wide width, horizontally extending portion, and narrower width, horizontally extending top and bottom portions, with the wide central portion connecting to the narrower top portion by a vertically extending, left of center portion, and connecting to the narrower bottom portion by a vertically extending, right of center portion.

[0043] Referring to the middle left bottom of Figure 2B, a second polysilicon conductor PC2 extends vertically downwardly to cross the M shaped region RX1 to form the gate of device P1, with the drain of P1 being formed in the M shaped active silicon region to the left of the gate, and the source of P1 being formed in the M shaped region to the right of the gate. The second polysilicon conductor PC2 also extends vertically upwardly to cross the bottom horizontally extending portion of the second region RX2 to form the gate of device N1, with the drain of N1 being formed in the bottom horizontally extending active silicon portion to the left of the gate, and the source of N1 being formed in the bottom horizontally extending portion to the right of the gate.

[0044] Referring to the middle right bottom of Figure 2B, a third polysilicon conductor PC3 extends vertically downwardly to cross the M shaped region RX1 to form the gate of device P2, with the drain of P2 being formed in the M shaped active silicon region to the right of the gate, and the source of P1 being formed in the M shaped region to the right of the gate. The third polysilicon conductor PC3 also extends vertically upwardly to cross the bottom horizontally extending portion of the second region RX2 to form the gate of device N2, with the drain of N2 being formed in the bottom horizontally extending active silicon portion to the right of the gate, and the source of N2 being formed in the bottom horizontally extending portion to the left of the gate. The third polysilicon conductor PC3 also extends further vertically upwardly to cross the middle horizontally extending portion of the second region RX2 to form the gate

of device N4, with the drain of N4 being formed in the middle horizontally extending active silicon portion to the right of the gate, and the source of N4 being formed in the middle horizontally extending portion to the left of the gate.

[0045] The SRAM 22 formed in the top portion of Figure 2B is formed symmetrically opposite to the SRAM 20 formed in the bottom portion of Figure 2B, with an inverted (relative to RX1) M shaped active silicon region RX3, and an inverted (relative to PC1) shallow U shaped fourth polysilicon conductor PC4, and inverted (relative to PC2, PC3) fifth and sixth polysilicon conductors PC5, PC6.

[0046] The XOR circuit 24 consisting of devices N3, N4, N5, N6 is formed in the central wide width, horizontally extending active silicon portion of the second region RX2. A vertically extending polysilicon conductor PC7 intersects the central horizontally extending portion to form the gate of device N5, and a vertically extending polysilicon conductor PC8 intersects the central horizontally extending portion to form the gate of device N6. The formations of the devices N3, N4 of the exclusive OR circuit 24 have already been discussed above.

[0047] The active silicon RX regions are surrounded by STI (shallow Trench Isolation), which prevents interferences of adjacent devices.

[0048] Figure 2B also illustrates the electrical connectors EC, which connect the different CAs (contacts) with M1 (first level metal).

[0049] Figure 2C shows the metal wiring of the design of Figure 2B, and shows first, second and third metal layers M1, M2, M3, connections to a power supply VDD, connections to ground GND, contacts CA, and vias V1, V2.

[0050] Figure 2D corresponds generally to Figure 2B and illustrates further details and dimensions of the new design in 0.13 um CMOS technology.

[0051] The beta ratio of a device is the ratio of the conductivity of the pull down device to the conductivity of the passgate device, and ~[m*(W/L)] of the pulldown device vs [m*(W/L)] of the passgate device, where m is the carrier mobility. For SRAM cell stability, the beta ratio is >=1.5. A higher beta ratio means better stability. If the passgate is a PFET device then the carrier mobility is half of the electron mobility of an NFET

passgate. Thus for the same layout, the beta ratio would be doubled when the NFET passgate is replaced by the PFET passgate. Or the pull down NFET can be reduced by one half to maintain the same beta ratio. The reverse beta ratio is 1/(beta ratio), as a metric for the write performance of the cell, noting that it is harder to write a more stable cell. In the CAM cell of the present invention, a reverse beta ratio of about 0.6 is provided in the layout to allow read/write operations with conventional support circuitry.

[0052] The present invention replaces the NFET passgates in a CAM cell by PFET SRAM passgates, which results in a 20% improvement in density (7.80 um2 vs 9.61 um2). The additional benefits of PFET passgates are better cell stability and lower power dissipation. The simple PFET passgate layout also allows more stable and cooler operation. The present invention provides a full ternary CAM cell wherein a data bit and a mask bit are included for actual product implementation.

[0053] While several embodiments and variations of the present invention for a content addressable memory with PFET passgate SRAM cells are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.